WHAT IS CLAIMED IS:

1. For use in a wide-issue pipelined processor, a mechanism for reducing pipeline stalls between conditional branches, comprising:

a mispredict program counter (PC) generator that generates a mispredict PC value for each conditional branch instruction in a pipeline of said processor; and

mispredict PC storage, coupled to said mispredict PC generator, that stores said mispredict PC value at least until a resolution of said conditional branch instruction occurs and makes said mispredict PC value available to a PC of said processor if said resolution results in a mispredict condition.

2. The mechanism as recited in Claim 1 wherein said mispredict PC generator is associated with a static branch predictor of said processor.

3. The mechanism as recited in Claim 1 wherein said mispredict PC generator generates a branch prediction and said mispredict PC value in a single clock cycle.

4. The mechanism as recited in Claim 3 wherein said branch prediction is employed to prefetch instructions.

5. The mechanism as recited in Claim 1 wherein a mispredict PC queue of said mispredict PC storage has at least as many slots as said pipeline has stages.

6. The mechanism as recited in Claim 1 wherein said mispredict PC value moves through registers of said mispredict PC storage as said conditional branch instruction moves through stages in said pipeline.

7. The mechanism as recited in Claim 1 wherein said resolution occurs in an execution stage of said pipeline.

8. The mechanism as recited in Claim 1 wherein said processor is a digital signal processor.

9. For use in a wide-issue pipelined processor, a method of reducing pipeline stalls between conditional branches, comprising:

generating a mispredict program counter (PC) value for each conditional branch instruction in a pipeline of said processor; and

storing said mispredict PC value at least until a resolution of said conditional branch instruction occurs; and

making said mispredict PC value available to a PC of said processor if said resolution results in a mispredict condition.

10. The method as recited in Claim 9 wherein said mispredict PC generator is associated with a static branch predictor of said processor.

11. The method as recited in Claim 9 wherein said generating is carried out in a single clock cycle, said method further comprising generating a branch prediction in a single clock cycle.

12. The method as recited in Claim 11 further comprising employing said branch prediction to prefetch instructions.

13. The method as recited in Claim 9 wherein a mispredict PC queue of said mispredict PC storage has at least as many slots as said pipeline has stages.

14. The method as recited in Claim 9 further comprising moving said mispredict PC value through registers in said mispredict PC storage as said conditional branch instruction moves through stages in said pipeline.

15. The method as recited in Claim 9 wherein said resolution occurs in an execution stage of said pipeline.

16. The method as recited in Claim 9 wherein said processor is a digital signal processor.

17. A digital signal processor, comprising:

a pipeline having stages capable of executing conditional branch instructions;

a wide-issue instruction issue unit;

a mispredict program counter (PC) generator that generates a mispredict PC value for each conditional branch instruction in said pipeline; and

mispredict PC storage, coupled to said mispredict PC generator, that stores said mispredict PC value at least until a resolution of said conditional branch instruction occurs and makes said mispredict PC value available to a PC of said DSP if said resolution results in a mispredict condition.

18. The DSP as recited in Claim 17 wherein said mispredict PC generator is associated with a static branch predictor in said instruction issue unit.

19. The DSP as recited in Claim 17 wherein said mispredict PC generator generates a branch prediction and said mispredict PC value in a single clock cycle.

20. The DSP as recited in Claim 19 wherein said branch prediction is employed to prefetch instructions.

21. The DSP as recited in Claim 17 wherein a mispredict PC queue of said mispredict PC storage has at least as many slots as said pipeline has said stages.

22. The DSP as recited in Claim 17 wherein said mispredict PC value moves through registers in said mispredict PC storage as said conditional branch instruction moves through said stages.

23. The DSP as recited in Claim 17 wherein said resolution occurs in an execution stage of said pipeline.